

# Design-driven Optimisation of a 90 nm RF CMOS Process by use of Elevated Source/Drain

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## Abstract

Ultra deep submicron CMOS is a promising technology for wireless applications. In order to obtain an optimal RF performance, many trade-offs can be made during the development of a CMOS technology that is traditionally driven by digital requirements. Using logic devices from a 90 nm digital CMOS technology node, RF models are generated that allow feedback from RF designs and optimisation of the technology for RF applications. As a case study, the elevated source drain (<sup>E</sup>S/D) architecture is optimised for RF performance. The influence of this process optimisation on an extrinsic reliability threat is investigated using Electro-Static Discharge (ESD) withstanding capability.

## 1. Introduction

Aggressive scaling of digital CMOS technology has validated CMOS technology as a good candidate for RF applications [1]. Typically, the CMOS technology development cycle for a particular technology node has a clear separation between the development of the core technology —for digital applications— and the subsequent development of the so-called technology options or modules. The latter includes, amongst others, the development and optimisation of specific devices and/or technology parameters for RF applications.

Based on an initial set of target specifications from the previous technology nodes, development starts on the front end of line process technology regarding device architecture and is limited to digital devices. In a second phase, typically 6 to 12 months later, a first physical and electrical design rule set is provided to (digital) designers, so that initial demonstrators and prototypes can be designed. Typically, the development of additional modules, e.g. for analog-RF devices, only starts after the basic digital technology specifications are frozen.

At the same time, the rapid downscaling of technologies along with process changes, could lead to changes in device reliability performance. One such major reliability concern is the Electrostatic Discharge induced device degradation. Conventionally, on-chip ESD protection circuits are developed to protect the device from ESD events. Technology scaling, coupled with the increasing ESD requirements, makes the realization of a robust ESD protection very difficult, especially in RFICs, where the ESD protection should not degrade the RF performance of the circuit.

In this paper, the results of the development of analog-RF modules *simultaneously* with the development of the digital CMOS technology are presented. This approach has two very important advantages: first, it shortens the overall technology development cycle for RF applications and thus the time-to-market; secondly, it gives the opportunity to introduce technology features beneficial for the optimisation of RF performance and ESD protection early in the technology development cycle.

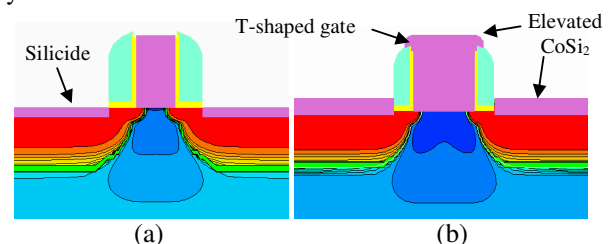


Fig. 1. TCAD cross-section of a transistor without (a) and with (b) Elevated Source/Drain (<sup>E</sup>S/D).

Many process variations are possible during silicon process optimisation. In this paper, an <sup>E</sup>S/D architecture (Fig. 1) is optimized with respect to RF performance and ESD reliability. <sup>E</sup>S/D architecture is beneficial for RF performance due to the reduction of gate sheet resistance caused by the T-shaped gate and the reduction of junction leakage [2] intrinsic to this device architecture.

No additional mask levels are required to implement this architecture.

Based on logic devices from the 90 nm CMOS node, described in section 2, initial RF models are extracted and presented (section 3). In section 4, simulation results from a 5 GHz low noise amplifier (LNA) are presented as a technology demonstrator that delivers feedback to the processing technology development.

## 2. Process Technology

NMOS and PMOS transistors were fabricated on p-type Silicon substrate in a 90 nm CMOS technology, with copper metal back-end. The RF potential of this high-performance technology has been explored earlier [3]: a cut-off frequency ( $f_T$ ) of 140 GHz was achieved and a maximum oscillation frequency ( $f_{max}$ ) of 320 GHz has been predicted.

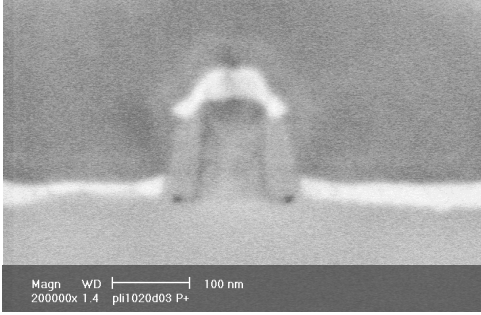


Fig. 2. Cross-section SEM of  $E^S/D$ : the source/drain silicide stops at the same level as the gate oxide and the spacer bottom. The selective epitaxially grown layer creates the T-shape formation on the poly gate.

The approach used to build an  $E^S/D$  architecture is to use Selective Epitaxial Growth (SEG) of silicon after source/drain implantation. The cobalt silicide layer is grown to a thickness that totally consumes the SEG layer [2][4] (see Fig. 2). Different S/D architectures are investigated: with and without Selective Epitaxial Growth (SEG), with 10 nm and 12 nm Co. A maximum exists for the SEG thickness and is limited by the bridging between the T-shaped gate polycide and the  $E^S/D$  SEG [5][6].

For the optimised device with  $E^S/D$  (having similar gate length), the transconductance ( $g_m$ ) and  $f_T$  of these devices are comparable with the best-published results [12][21], see Fig. 3. However,  $f_{max}$  is comparatively low (60 GHz) due to the high effective gate resistance, which in turn is caused by a non-optimised transistor layout, namely a 2-gate fingered structure [8]. This can simply be improved by using more gate fingers, thus reducing the gate resistance.

To optimise this architecture for RF, however, it is important to note that the overall RF circuit performance must be considered in addition to  $f_T$  and  $f_{max}$ , and will be discussed in section 4.

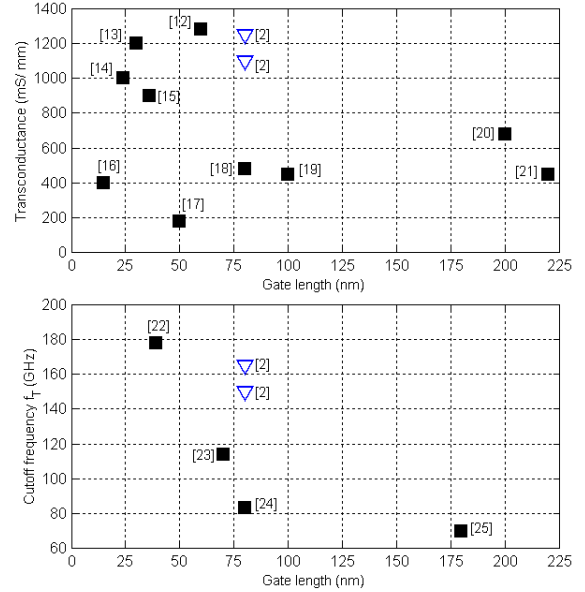


Fig. 3. The technology used in this study ( $\nabla$ ) can compete with the state-of-the-art devices ( $\blacksquare$ ) in terms of transconductance (top) and cut-off frequency (bottom).

## 3. RF modelling

The initial RF model parameters are extracted from the unfrozen digital transistors based on a compact MOS Model 'MOS model 11' (MM11) [7]. MM11 is used for the intrinsic transistor. This model is based on a continuous description of the surface potential throughout all operation regimes, including the increasingly important moderate inversion regime. The external gate resistance, source/drain capacitances, and substrate network are not included in this model, instead they are modelled separately.

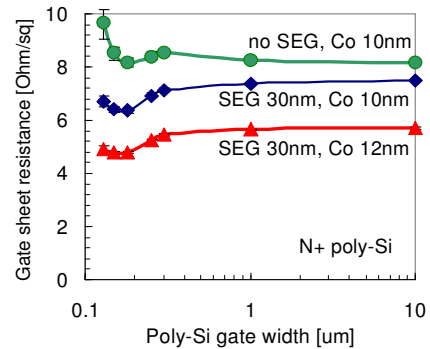


Fig. 4. Gate sheet resistance versus poly line width for different  $E^S/D$  architectures.

The gate sheet resistance as a function of the polysilicon line width is extracted from measurements for different  $E^S/D$  architectures, shown in Fig. 4. RF designers typically use a folded two sided gate contact transistor layout (see Fig. 5) in order to lower the gate resistance. Therefore, an appropriate scalable model for the gate resistance and junction capacitances must be implemented. The substrate network is dependent on the RF transistor layout. Since dedicated test structures are not available at present, the substrate resistances are estimated and modelled according to the previous

technology node. Using this RF model, RF design and Process optimisation is discussed in the next section.

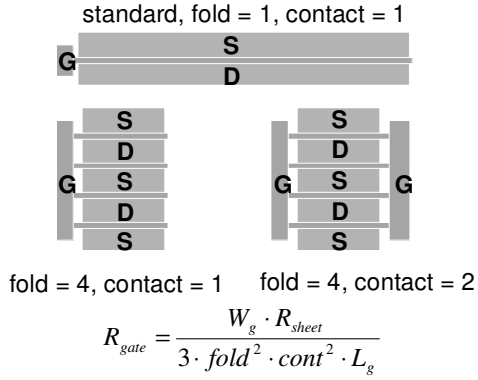


Fig. 5. Folded two-sided gate contact transistor layout to lower the gate resistance ( $R_{gate}$ ).

Preliminary  $f_{max}$  measurements on an 8-double-contacted gate finger device (35 nm SEG and 12 nm Co) show an improvement of  $f_{max}$  up to 108 GHz. However, the thicker oxide of 2.2 nm (used for digital application with low standby power) results in a decrease of  $f_T$  (78 GHz), Fig. 6.

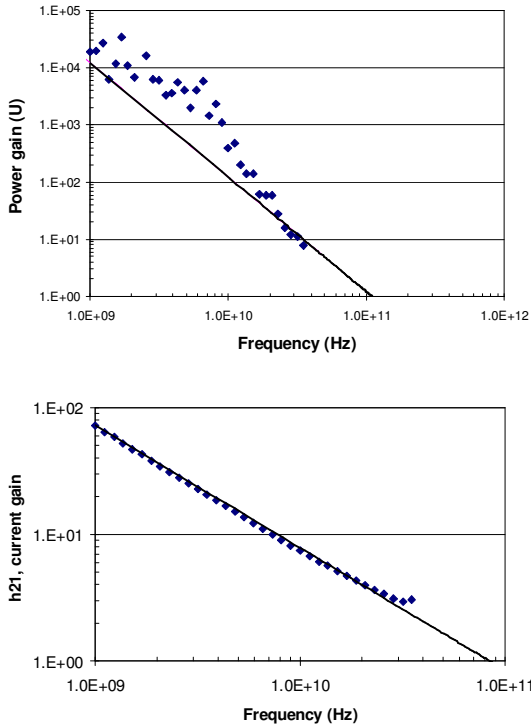


Fig 6.  $f_{max}$  measurement (top) and  $f_T$  measurement (bottom) for a device with 2.2 nm oxide thickness (35 nm SEG and 12 nm Co).

#### 4. RF design & Process Optimisation

A fully integrated 5 GHz low noise amplifier (LNA) with a 1.2 Volt supply voltage is simulated to demonstrate the impact of the  $E^S/D$  architecture on the noise performance of the circuit with and without ESD

protection (Fig. 7). Further, the influence of  $E^S/D$  on the ESD withstanding capability is studied.

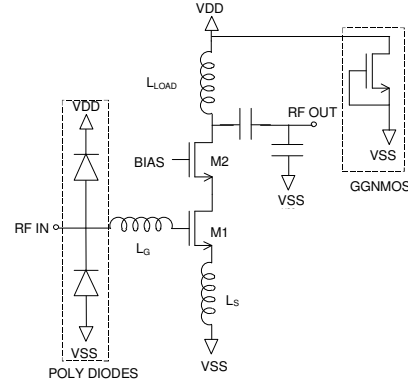


Fig. 7. A fully integrated 5 GHz Low Noise Amplifier with optional ESD protection: poly diodes and grounded gate NMOS (ggNMOS).

#### A. Impact of elevated source/drain on the noise performance of an LNA

The LNA consists of an inductively degenerated stage with transistor M1, followed by a common gate stage M2. The objective of the LNA design is to obtain a low noise figure (NF) at a low current consumption. To design the circuit, the power-constrained noise-optimisation method [9] is used. M1 has an aspect ratio, W/L, of 112  $\mu\text{m}/90\text{ nm}$  and it operates in moderate inversion with a drain current of 1 mA. This transistor is simulated as having 14 fingers in order to reduce the gate resistance.

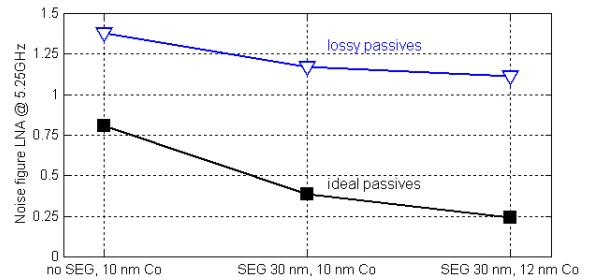


Fig. 8. Simulations of a 5 GHz LNA show a substantial improvement of the Noise Figure (NF) for the  $E^S/D$  device. Increasing Co thickness from 10 to 12 nm marginally improves the NF.

The noise simulation results, Fig. 8, clearly show a substantial improvement of the NF for the  $E^S/D$  device, compared to the non- $E^S/D$  device (due to the reduction of the gate sheet resistance). However, increasing Co thickness from 10 to 12 nm marginally improves the NF since the transistor-generated noise is then lower than the noise from the input inductor. Thus, noise in an RF CMOS LNA is dominated by the contribution of the passive elements and not by the contribution of the transistors.

## B. Electrostatic discharge (ESD) reliability

Process technology optimisation for RF performance might be conflicting with ESD requirements and therefore has to be examined. For the same three process variations (no SEG 10 nm Co, 30 nm SEG 10 nm Co, 30 nm SEG 12 nm Co), ESD stress tests (using Transmission Line Pulsing (TLP)) [10] have been performed on grounded-gate NMOS (ggNMOS) and on poly diodes. The ggNMOS has a  $0.45\ \mu\text{m}$  gate length and  $50\ \mu\text{m}$  width, the poly diode is in an nwell with a  $0.1\ \mu\text{m}$  poly length and  $20\ \mu\text{m}$  width.

The measurements clearly show the benefit of using  $E^S/D$  with 30 nm of SEG and 10 nm of Co for the ggNMOS as well as for the poly diodes (Fig. 9). Further increase of the Co thickness degrades the ESD robustness.

From these two-terminal ESD structures, the RF parasitic behaviour for a ggNMOS and poly diode, with same ESD robustness, is modelled as an RC equivalent circuit [11], and their impedance is shown in Fig. 10. Poly diodes have a smaller parasitic capacitance than the ggNMOS for the same ESD protection level. Hence, they are used for the RF-input protection of the LNA (Fig. 7). The ggNMOS is used as the power supply protection. The influence of the different  $E^S/D$  architectures on the equivalent capacitance is negligible (Fig. 10).

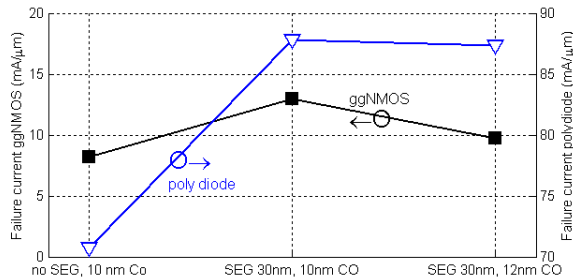


Fig. 9. ESD data on ggNMOS (grounded gate NMOS) and poly diodes, clearly showing the improvements using SEG 30 nm, 10 nm Co for ESD.

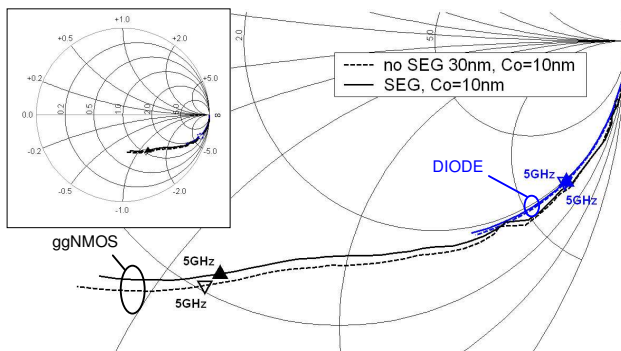


Fig. 10. Poly diodes have smaller parasitic capacitance than ggNMOS. Different  $E^S/D$  architectures marginally influence the impedance of the protection devices.

The degradation of the RF performance (see Table I) caused by the ESD protection is examined by simulation. From the maximum allowable performance degradation, an upper limit for the size of the two poly diodes is derived. In this case, a width of  $15\ \mu\text{m}$  is chosen, which provides 2 kV HBM ESD robustness.

Table I Influence of ESD Protection on the RF Performance of the 5 GHz LNA

	Without ESD	With ESD
S21	13.18 dB	12.75 dB
S11	-26.45 dB	-14.47 dB
NF	1.48 dB	1.9 dB

## 5. Conclusions

To accelerate the development of an ultra deep submicron process for RF applications, the simultaneous development of the digital CMOS technology and the analog-RF modules is proposed. The RF requirements are determined using RF circuit simulations with models extracted from an early prototype silicon process run. To illustrate this approach, this paper has discussed the development of an elevated source and drain architecture and its optimisation. Together with circuit design requirements, reliability tests such as ESD measurements provide an additional feedback to process technology. In this way, an optimal thickness of the Cobalt (Co) layer in the elevated source/drain architecture (30 nm SEG of Silicon with 10 nm Cobalt for our 90nm CMOS technology) in an early phase of the development is determined and additional expensive process iterations are avoided.

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